JEDEC STANDARD

Single Pulse Unclamped Inductive Switching (UIS) Avalanche Test Method

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SINGLE PULSE UNCLAMPED INDUCTIVE SWITCHING (UIS) AVALANCHE TEST METHOD

(From JEDEC Council Ballot JCB-89-49, formulated under the cognizance of JC-25 Committee on Transistors and Intelligent Power Devices.)

1. PURPOSE

This method describes a means for testing the ability of a power switching device to withstand avalanche breakdown.

2. SCOPE

The approach outlined in this document may be applied to MOS and IGBT devices, both N and P type. The text of this method focuses on enhancement-mode field effect transistors.

3. INTRODUCTION

This test simulates a single event stress that a device may encounter in the off-state. It has been reported in the literature that catastrophic device failure is triggered by a combination of T_J and I_D for a power MOS device. Failure can be initiated by turn-on of the parasitic bipolar present in a vertical DMOS device or by a thermally induced mesoplasma formation. The test is defined when T_J (starting) and $i_D(t)$ are specified.

4. SYMBOLS AND DEFINITIONS

I_{as}	-	The peak current reached during device avalanche.
t_{av}	-	The time duration of device avalanche.
L	-	Inductance.
R	-	Resistance.
V_{DD}	-	The output circuit supply voltage.
$V_{DSX(sus)}$	-	The effective (constant) device breakdown voltage during avalanche. The instantaneous device breakdown voltage will change with junction temperature during a test. $V_{DSX(sus)}$ is determined for an inductive circuit by measuring t_{av} and calculating its value.

5. TEST CIRCUIT

Figure 1 is the test circuit schematic. The DUT is turned on ramping the drain current to a desired value. The DUT is turned off allowing the device to sustain avalanche. The circuit waveforms are illustrated in Figure 2. The time in avalanche is related to circuit parameters and the device $V_{DSX(sus)}$ as follows:

$$t_{av} = (L/R) \ln [I_{as}R/(V_{DSX(sus)}-V_{DD}) +1], \text{ if } R > 0$$

$$t_{av} = (LI_{as}/(V_{DSX(sus)}-V_{DD}), \text{ if } R = 0$$

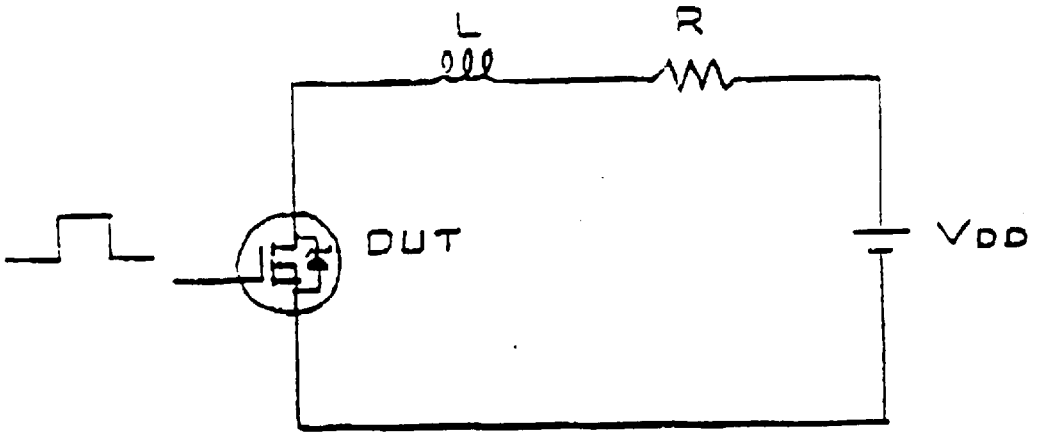

Figure 1
Test Circuit Schematic

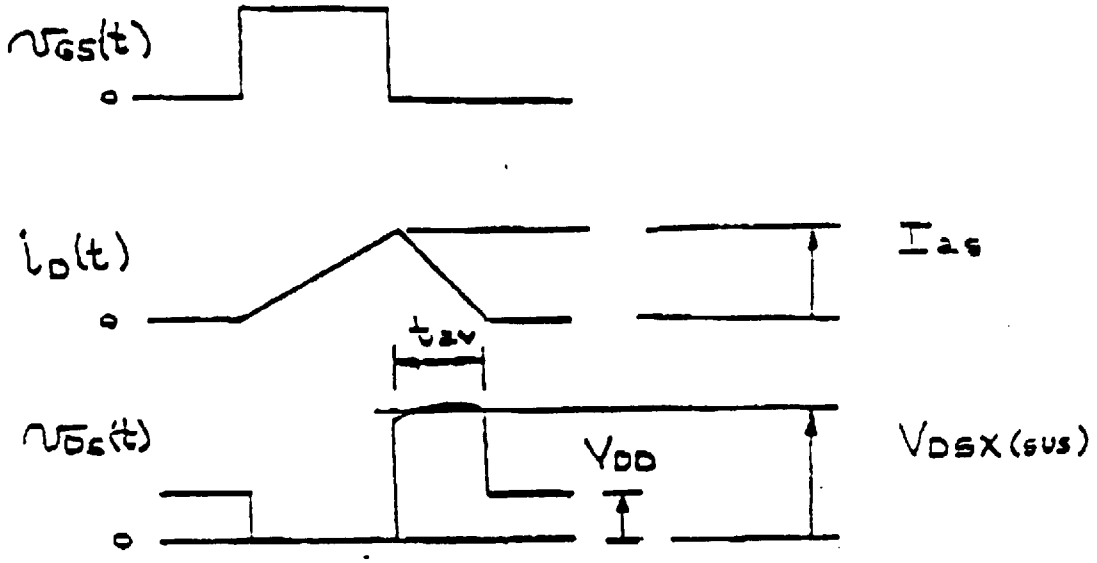

Figure 2
Circuit Waveforms

6. REQUIREMENTS

The following must be specified:

(1) T_J - Starting Junction Temperature

(2) $i_D(t)$ - Current/Time Waveform

Inductive $i_D(t)$ is specified by the following:

a) I_{as} - peak avalanche current

b) L - load inductance

c) R - load resistance

d) V_{DD} - supply voltage

(3) t_{av} - Measurement of t_{av} is optional. Its value varies with device $V_{DSX(sus)}$.

(4) Turn-off gate drive conditions (for example V_{GS} = 0 volts, R_{GS} = 25 ohms).

Limits, values, tolerances and rating curves are the province of the Registration Data Format and associated JEDEC Standards.

7. TEST FAILURES

Test failures are defined as those devices which:

a) Fail catastrophically.

b) Exhibit a V_{DS} collapse below the device $V_{(BR)DSS}$ rated voltage during avalanche.

c) Exhibit higher than specified I_{DSS} or I_{GSS} leakage current after the test.


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